Listing of Claims:

Claim 1. (Previously Presented) A computer system comprising:

a processor;

a memory unit configured to store data used by the processor;

a memory control unit configured to manage data flowing into and out of the memory unit; and

a circuit board comprising:

at least two layers formed in parallel to a surface of said circuit board,

a first signal line, formed on a first layer of the circuit board and connected between a first pin on the memory unit and the memory control unit, and

a second signal line also formed on the first layer of the circuit board and connected to the first pin on the memory unit, a first portion of the second signal line at an acute angle relative to a first portion of the first signal line, a second portion of the second signal line substantially parallel to a second portion of the first signal line,

wherein said first layer defines a non-grounded gap between said first and second portions of the first and second lines.

Claim 2. (Canceled)

Claim 3. (Original) The system of claim 1, further comprising third and fourth signal lines, on a second layer of the circuit board, different than the first layer.

Claim 4. (Previously Presented) The system of claim 1, wherein the second portion of the first signal line and the second portion of the second signal line have substantially equal widths.

Claim 5. (Previously Presented) The system of claim 4, wherein the second portion of the first signal line and the second portion of the second signal line are separated by a perpendicular distance substantially equal to said widths.

Claim 6. (Currently Amended) The system of claim 5, wherein the widths of the lines and the perpendicular distance separating the second portions of the lines are each substantially equal to 5 mils.

Claim 7. (Previously Presented) The system of claim 1, wherein the memory unit comprises a RAMBUS™ device.

Claim 8. (Previously Presented) A method for use in routing signals between a memory unit and a memory control unit, the method comprising:

delivering a first signal over a first signal line on a first layer formed in parallel to a second layer on a surface of

a multi-layer circuit board and connected between the memory control unit and a first pin on the memory unit;

delivering a second signal over a second signal line formed on the first layer of the circuit board and connected to the first pin of the memory unit, a first portion of the second signal line formed at an acute angle relative to a first portion of the first signal line, a second portion of the second signal line formed substantially parallel to a second portion of the first signal line,

said first and second portions of the first and second signal lines separated without a ground connection therebetween.

Claim 9. (Canceled)

Claim 10. (Previously Presented) The method of claim 8, further comprising delivering another signal to said memory control unit on another parallel layer of the circuit board over portions of the first and second signal lines that are not separated by any conductive traces.

Claim 11. (Previously Presented) The method of claim 8, wherein delivering the first signal and the second signal includes delivering the signals over second portions of the first and second signal lines that have substantially equal widths.

Claim 12. (Previously Presented) The method of claim 11, wherein delivering the first signal and the second signal includes delivering the signals over second portions of the first and second signal lines that are separated by a perpendicular distance substantially equal to their widths.

Claim 13. (Previously Presented) The method of claim 12, wherein delivering the first signal and the second signal includes delivering the signals over second portions of the first and second signal lines that are substantially equal to 5 mils wide and that are separated by a perpendicular distance substantially equal to 5 mils.

Claim 14. (Previously Presented) A method for use in manufacturing a computer system, the method comprising:

forming at least two layers parallel to a surface of a circuit board, with first and second signal lines on a first layer of the board;

connecting a memory unit to the board such that a first pin on the memory unit connects to the first and second signal lines;

affixing a memory control unit to the board such that the memory control unit connects to at least the first signal line;

forming a first portion of the second signal line to be at an acute angle relative to a first portion of the first signal

line; and

forming a second portion of the second signal line to be substantially parallel to a second portion of the first signal line.

Claim 15. (Canceled)

Claim 16. (Previously Presented) The method of claim 14, further comprising forming the first and second signal lines such that no conductive trace lies between the second portion of the first signal line and the second portion of the second signal line.

Claim 17. (Previously Presented) The method of claim 16, further comprising forming the second portion of the first signal line and the second portion of the second signal line to have substantially equal widths.

Claim 18. (Previously Presented) The method of claim 17, further comprising forming the second portion of the first signal line and the second portion of the second signal line to be separated by a perpendicular distance approximately equal to their widths.

Claim 19. (Previously Presented) The method of claim 18, further comprising forming the signal lines such that the widths of the lines and the perpendicular distance separating the

second portions of the lines are all substantially equal to 5 mils.

Claim 20. (Previously Presented) A circuit board comprising at least two layers formed in parallel to a surface of said circuit board for use in a computer system comprising:

a memory unit;

a memory control unit; and

a data bus connecting the memory control unit to the memory unit and comprising:

a first signal line formed on a first layer of the circuit board and connected to the memory control unit and to a first pin on the memory unit, and

a second signal line formed on the first layer of the circuit board and also connected to the first pin connection on the memory unit, a first portion of the second signal line at an acute angle relative to a first portion of the first signal line, a second portion of the second signal line substantially parallel to a second portion of the first signal line,

wherein the widths of the lines and a perpendicular distance separating the second portions of the lines are each substantially equal, and

wherein said first layer defines a non-grounded gap between said first and second portions of the first and second lines.

Claims 21-22. (Canceled)

Claim 23. (Previously Presented) The computer system of claim 1, wherein the memory unit comprises a memory repeater hub.

Claim 24. (Previously Presented) The circuit board of claim 20, wherein the memory unit comprises a memory repeater hub.